PATENT ABSTRACTS OF JAPAN

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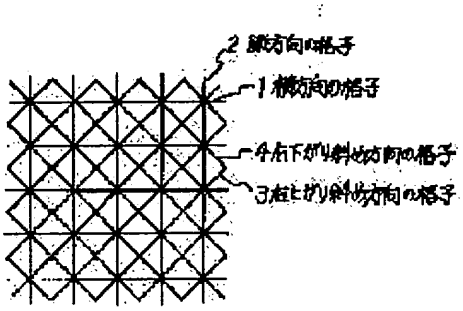
(72)Inventor : SATO AKIHIRO

(54) AUTOMATIC LAYOUT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:

PURPOSE: To make the length of wiring short by a method wherein, in addition to wiring layer which is used for wiring on lattices in the transverse and longitudinal directions in conventional cases, a wiring layer which is used for lattice-shaped wiring in the oblique direction is used.

CONSTITUTION: In addition to lattices 1 in the transverse direction and lattices 1 in the longitudinal direction, lattices 3 in the rightward ascending oblique direction and lattices 4 in the rightward descending oblique direction are set, they are used as wiring layers which are used mainly for wiring on the respective lattices 1, 2, 3, 4, and a first inter-connection layer to a fourth wiring layer are allotted. Thereby, the length of the wiring can be shortened to 0.7 times at the most, and the wiring resistance and wiring capacitance are reduced. As a result, the operating speed of the title integrated circuit can be made fast.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The automatic-layout approach of the semiconductor integrated circuit characterized by using the wiring layer used for wiring on at least one lateral grid, the wiring layer used for wiring on at least one grid of a lengthwise direction, and the wiring layer used for wiring on at least one grid of the direction of slant.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the automatic-layout approach using the algorithm which wires by the wiring layer which was able to appoint the decided grid top about the automatic-layout approach of a semiconductor integrated circuit.
[0002]
[Description of the Prior Art] As shown in drawing 3 , the automatic-layout approach of the semiconductor integrated circuit using the algorithm which wires by the wiring layer which was able to appoint the grid top the former was decided to be mainly used the 1st wiring layer for wiring on the lateral grid 11, and mainly used the 2nd wiring layer for wiring on the grid 12 of a lengthwise direction. Furthermore, it used like [when / when using the wiring layer of three or more layers / the 3rd wiring layer is called grid 11 top of the same longitudinal direction as the 1st wiring layer, and / the 4th wiring layer] the grid 12 top of the same lengthwise direction as the 2nd wiring layer, having assigned one by one.
[0003] Drawing 4 is the pattern Fig. which actually wired according to the grid of drawing 3 . In drawing 4 , the 1st wiring layer 15 is in a longitudinal direction, the 2nd wiring layer 16 is in a lengthwise direction, and it connects electrically by the connection pattern 17 of each wiring layers 15 and 16. These are the wiring patterns for carrying out electrical installation between A, a B point, C, and D point.
[0004]
[Problem(s) to be Solved by the Invention] By such automatic-layout approach of the conventional semiconductor integrated circuit, since it wired only on the grid 11 of a longitudinal direction or a lengthwise direction, and 12 even if it used the wiring layer of three or more layers, the die length of wiring had the trouble that there was nothing, only by becoming easy to carry out wiring, even if it increases a wiring layer, if it was short **** not much.
[0005] The purpose of this invention solves said trouble and is to offer the automatic-layout approach of a semiconductor integrated circuit of short-****(ing) the die length of wiring.
[0006]
[Means for Solving the Problem] The configuration of the automatic-layout approach of the semiconductor integrated circuit of this invention is characterized by using the wiring layer used for wiring on at least one lateral grid, the wiring layer used for wiring on at least one grid of a lengthwise direction, and the wiring layer used for wiring on at least one grid of the direction of slant.
[0007]
[Example] Drawing 1 is a wiring grid Fig. used in the one example of this invention. In drawing 1 , in addition to the lateral grid 1 and the grid 2 of a lengthwise direction, the grid 3 and the lower right of the direction of upward-slant-to-the-right slant set up the grid 4 of the ** slanting direction, and assign the 1st to 4th wiring layer as each grid 1, 2, and 3 and a wiring layer mainly used for wiring on four.
[0008] Drawing 2 is the pattern Fig. which performed the wiring pattern using the grid Fig. of drawing

1 .
[0009] In drawing 2 , there are the 1st wiring layer 7, the 2nd wiring layer 8, the 3rd wiring layer 5, and the 4th wiring layer 6, and the connection pattern 9 between each wiring layer is formed at the node etc.
[0010] the example which wired between A point B points and between C point D points in drawing 2 -- conventional drawing 4 -- comparing -- the die length of wiring -- 0.7 to 0.8 times -- short -- it is that it is ******.
[0011]
[Effect of the Invention] the wiring layer which uses this invention for wiring on the conventional width and the grid of a lengthwise direction as explained above -- in addition, since the die length of wiring can be short-****(ed) a maximum of 0.7 times and wiring resistance and wiring capacity become less by using the wiring layer used for wiring on the grid of the direction of slant, it has the effectiveness that a working speed becomes quick.

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TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the automatic-layout approach using the algorithm which wires by the wiring layer which was able to appoint the decided grid top about the automatic-layout approach of a semiconductor integrated circuit.

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PRIOR ART

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EFFECT OF THE INVENTION

[Effect of the Invention] the wiring layer which uses this invention for wiring on the conventional width and the grid of a lengthwise direction as explained above -- in addition, since the die length of wiring can be short-****(ed) a maximum of 0.7 times and wiring resistance and wiring capacity become less by using the wiring layer used for wiring on the grid of the direction of slant, it has the effectiveness that a working speed becomes quick.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By such automatic-layout approach of the conventional semiconductor integrated circuit, since it wired only on the grid 11 of a longitudinal direction or a lengthwise direction, and 12 even if it used the wiring layer of three or more layers, the die length of wiring had the trouble that there was nothing, only by becoming easy to carry out wiring, even if it increases a wiring layer, if it was short **** not much.
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MEANS

[Means for Solving the Problem] The configuration of the automatic-layout approach of the semiconductor integrated circuit of this invention is characterized by using the wiring layer used for wiring on at least one lateral grid, the wiring layer used for wiring on at least one grid of a lengthwise direction, and the wiring layer used for wiring on at least one grid of the direction of slant.

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EXAMPLE

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the wiring grid Fig. used by the automatic-layout approach of the semiconductor integrated circuit of one example of this invention.
[Drawing 2] It is the wiring pattern Fig. created along with the grid of drawing 1 .
[Drawing 3] It is the wiring grid Fig. used by the conventional automatic-layout approach.
[Drawing 4] It is the wiring pattern Fig. created along with the grid of drawing 3 .
[Description of Notations]
1 11 Lateral grid
2 22 Grid of a lengthwise direction
3 Grid of the Direction of Upward-Slant-to-the-Right Slant
4 Lower Right is Grid of the ** Slanting Direction.
5, 6, 15, 16 Wiring pattern for two points

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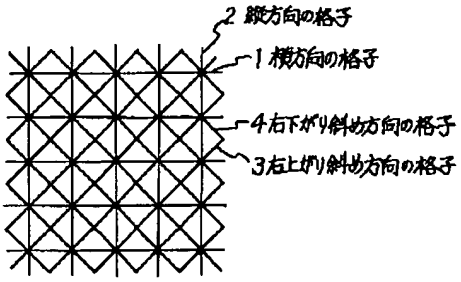
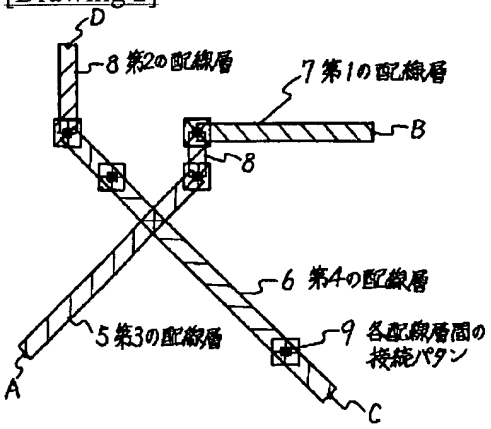
DRAWINGS

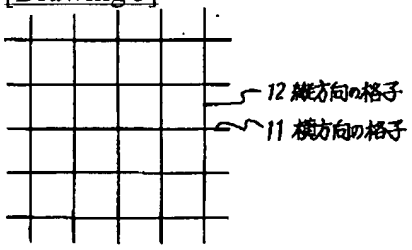
[Drawing 1]



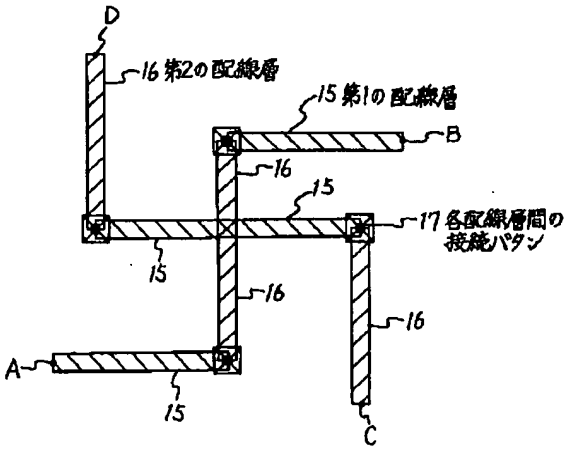
[Drawing 2]



[Drawing 3]



[Drawing 4]



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